Semiconductors

AN10001_6

ISP110x Interfacing

Rev. 06.00 — 12 April 2004 **Application note**

Document information

Info	Content
Keywords	ISP1102, ISP1104, ISP1105, ISP1106, USB, universal serial bus, transceiver
Abstract	This document demonstrates interfacing of the ISP110x transceivers. **Note**: ISP110x denotes the ISP1102, ISP1104, ISP1105 and ISP1106 Philips Advanced Universal Serial Bus transceivers, and any future derivatives.

PHILIPS

Revision history

Rev	Date	Description
6.0	Mar 2004	Removed ISP1107
5.0	May 2003	Added further content on HVQFN package
4.0	March 2003	• Removed ISP1103 interfacing • Inserted new HVQFN packaging for ISP1102/4/5
3.0	Oct 2002	Added the ISP1102 interfacing.
2.0	June 2002	Added the ISP1103 and ISP1104 interfacing.
1.0	Feb 2002	Known as "ISP1105/06/07 Interfacing Application Note"

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Contents

Note: ISP110x denotes the ISP1102, ISP1104, ISP1105 and ISP1106 Philips Advanced Universal Serial Bus transceivers, and any future derivatives.

1. Introduction

The ISP110x product family consists of the ISP1102, ISP1104, ISP1105 and ISP1106 Universal Serial Bus (USB) transceivers that are ideal for use in portable electronic devices, such as digital still cameras, personal digital assistants (PDAs) and mobile phones, in which power consumption in critical.

This document will demonstrate interfacing of the ISP110x transceivers.

2. ISP1102

2.1. Features of the ISP1102

- Compliant with ***Universal Serial Bus Specification Rev. 2.0***.
- Can transmit and receive USB data at full-speed (12 Mbit/s) only.
- Supports I/O voltage range from 1.65 V to 3.6 V.
- Has an integrated 5 V-to-3.3 V voltage regulator for powering through USB V_{BUS}.
- V_{BUS} presence indication on the VBUSDET pin.
- The RCV output is stable during SE0.
- The VP and VM pins function in the bidirectional mode allowing pin count saving for the ASIC interface.
- Low-power consumption.
- Supports ±12 kV ESD protection at the D+, D–, $V_{CC(5.0)}$ and GND pins.
- Available in HBCC16 and HVQFN14 halogen-free and lead-free packages.
- In the sharing mode, $V_{CC(I/O)}$ is connected, and $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are not connected. In this mode, the D+ and D– pins are made three-state, and the ISP1102 allows external signals of up to 3.6 V to share the D+ and D– lines. Its internal circuits ensure that virtually no current (maximum 10 A) is drawn through the D+ and D– lines. The power consumption through the $V_{CC(I/O)}$ and $V_{CC(5.0)}$ pins drop to the low-power state level. To indicate this mode, the VBUSDET and RCV pins are driven LOW.
- The ISP1102 can be used in the bypass mode (with +3.3 V on $V_{CC(5.0)}$) and also in the bus-power mode (with +5 V or V_{BUS} line on $V_{CC(5.0)}$).
- During suspend, the VBUSDET pin will be pulled HIGH.

2.2. Interfacing the ISP1102 to a System ASIC

Figure 2-1 shows a typical circuitry of an upstream connection with the ISP1102W in the bidirectional differential mode under the normal mode.

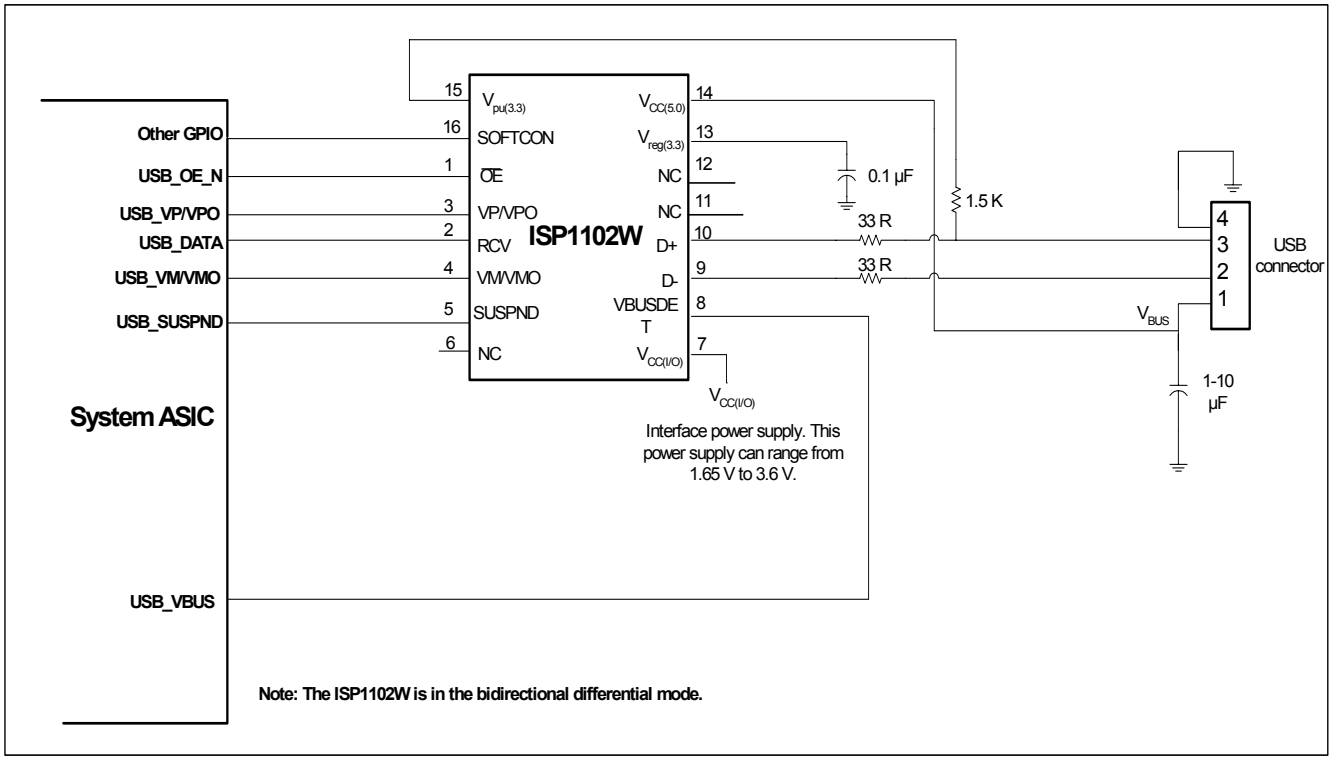

Figure 2-1: Upstream Connection with the ISP1102W in the Differential Mode under the Normal Mode

The upstream port connection can be done by pulling up the 1.5 kΩ resistor on D+ and D– by using $V_{pu(3.3)}$. Use the SOFTCON pin to enable or disable the pull-up.

$V_{CC(I/O)}$ is provided by the backend, FPGA or general microcontroller board circuitry. This voltage can range from 1.65 V to 3.6 V.

Figure 2-2 shows a typical schematic of an upstream connection circuitry with the ISP1102W in the differential mode under the bypass mode.

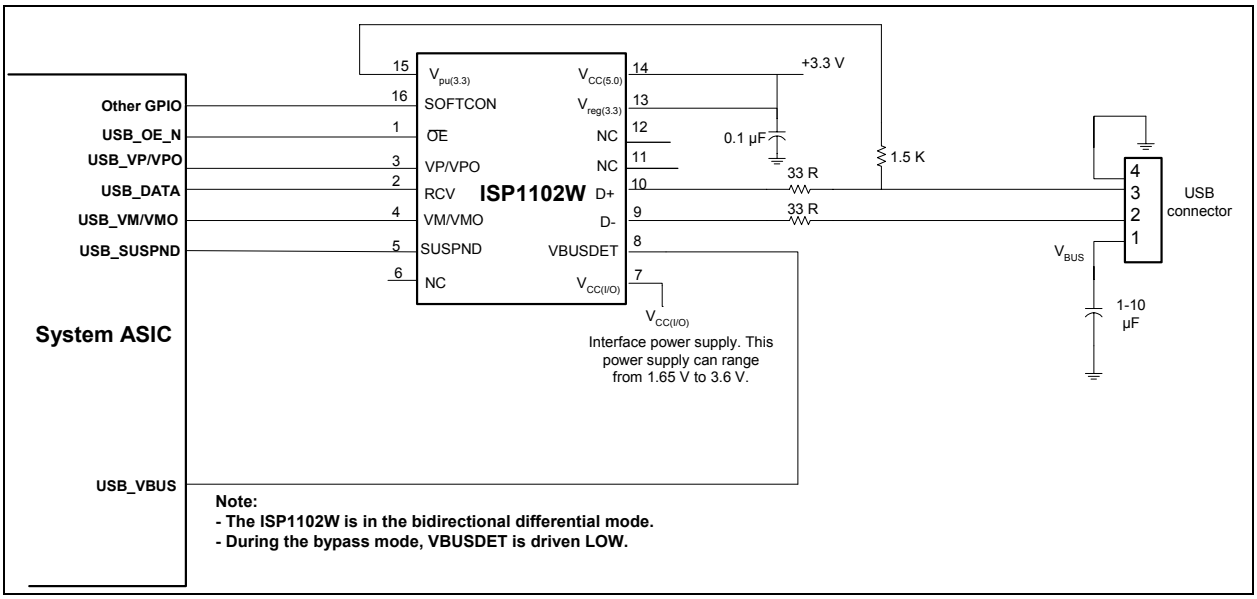

Figure 2-2: Upstream Connection with the ISP1102W in the Differential Mode under the Bypass Mode

For the downstream port connection, leave $V_{pu(3.3)}$ open. There is no 1.5 kΩ pull-up resistor from the D+ and D– lines to $V_{pu(3.3)}$. There are, however, two 15 kΩ termination resistors from the D+ and D– lines to GND (LOW). To reduce power consumption, connect the SOFTCON pin to GND.

A typical schematic of a downstream connection with the ISP1102W in the differential mode under the normal mode is given in Figure 2-3.

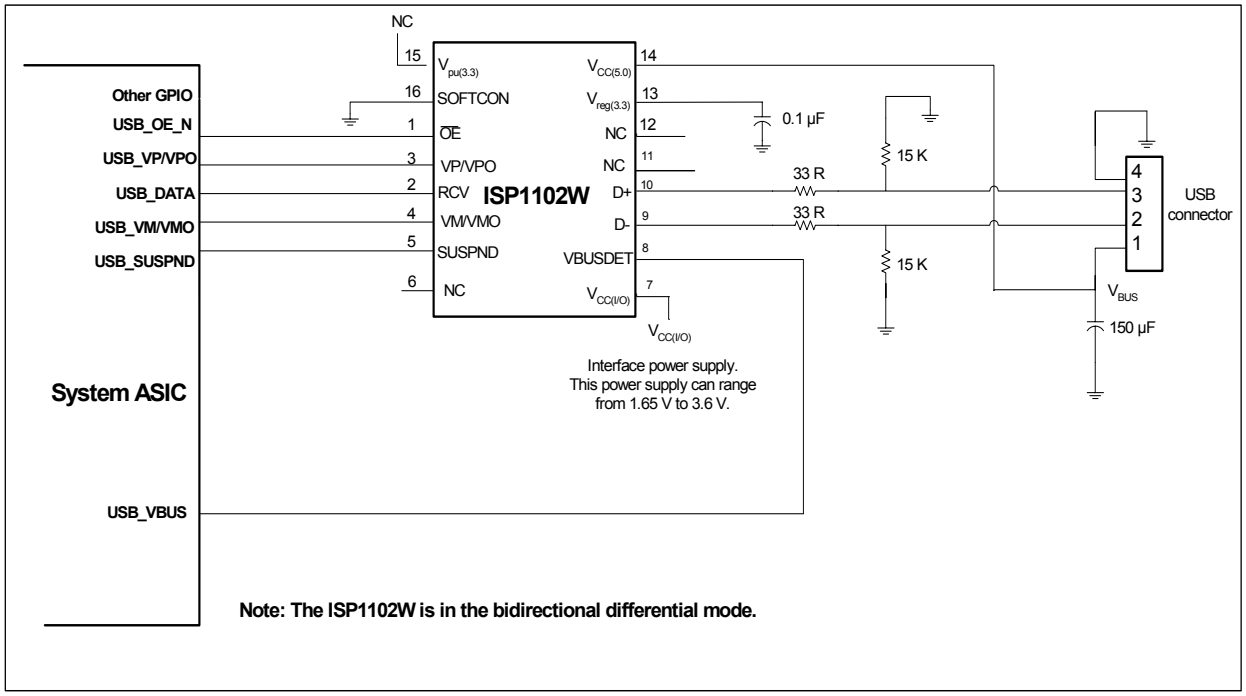

Figure 2-3: Downstream Connection with the ISP1102W in the Differential Mode under the Normal Mode

Figure 2-4 shows a typical circuitry of a downstream connection with the ISP1102 in the differential mode under the bypass mode.

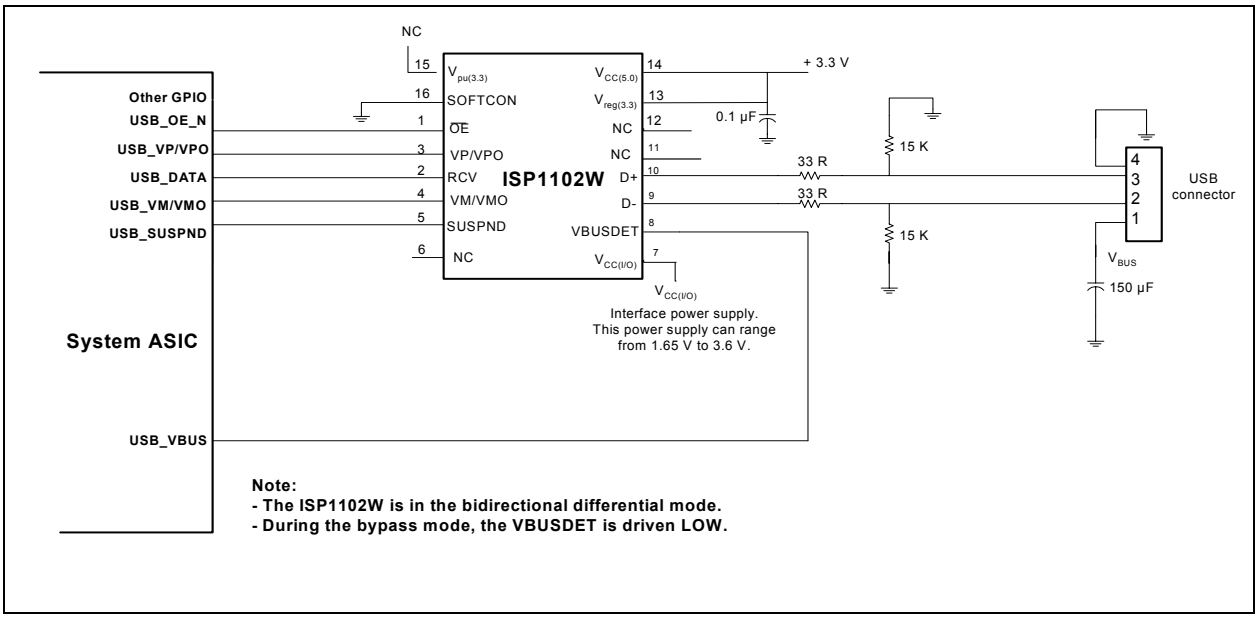

Figure 2-4: Downstream Connection with the ISP1102W in the Differential Mode under the Bypass Mode

Figure 2-1 to Figure 2-4 provide the connection circuitry for the ISP1102W (HBCC16) package. If you are using the ISP1102BS (HVQFN14) package in your application, see Table 2-1 for the pin assignment.

Table 2-1: Pin Assignment for the ISP1102BS Package

Pin No	ISP1102BS
1	$\overline{OE}$
2	RCV
3	VP/VPO
4	VM/VMO
5	SUSPND
6	$V_{CC(I/O)}$
7	VBUSDET
8	D–
9	D+
10	TEST_LOW or GND
11	$V_{reg(3.3)}$
12	$V_{CC(5.0)}$
13	$V_{pu(3.3)}$
14	SOFTCON
15	—
16	—

3. ISP1104

3.1. Features of the ISP1104

- Compliant with ***Universal Serial Bus Specification Rev. 2.0.***
- Can transmit and receive USB data at full-speed (12 Mbit/s) only.
- Supports I/O voltage range from 1.65 V to 3.6 V.
- Has an integrated voltage detector to detect the presence of the V_{BUS} ($V_{CC(5.0)}$) voltage. When V_{BUS} is lost, the D+ and D– pins can be shared with other serial protocols.
- The MODE input pin allows selection between the single-ended and differential input modes.
- Available in HBCC16 and HVQFN16 halogen-free and lead-free packages. The pin assignment for the two packages is the same.
- To make the ISP1104 termination compatible with the USB 2.0 requirements, the CMOS driver is designed to make its output impedance more process stable. This reduces unmatched termination; thereby reducing potential rings and undershoots.
- Contains a VBUSDET pin, which is a V_{BUS} output indicator (CMOS level with respect to $V_{CC(I/O)}$). When V_{BUS} is greater than 4.1 V, output is HIGH; and when V_{BUS} is lower than 3.6 V, output is LOW.
- In the sharing mode, $V_{CC(I/O)}$ is connected and $V_{CC(5.0)}$ is below 3.6 V. In this mode, the D+ and D– pins are made three-state and the ISP1104 allows external signals of up to 3.6 V to share the D+ and D– lines. Its internal circuits ensure that virtually no current (maximum 10 A) is drawn through the D+ and D– lines. The power consumption through the $V_{CC(5.0)}$ pin drops

to the low-power (suspend) state level. The VP and VM pins are driven HIGH, and the VBUSDET and RCV pins are driven LOW to indicate this mode.

- The ISP1104 is targeted for use in the bus-powered mode only (with +5 V or V_{BUS} line on $V_{CC(5.0)}$).

3.2. Interfacing the ISP1104 to a System ASIC

A typical schematic of the upstream connection with the ISP1104 in the single-ended mode is given in Figure 3-1.

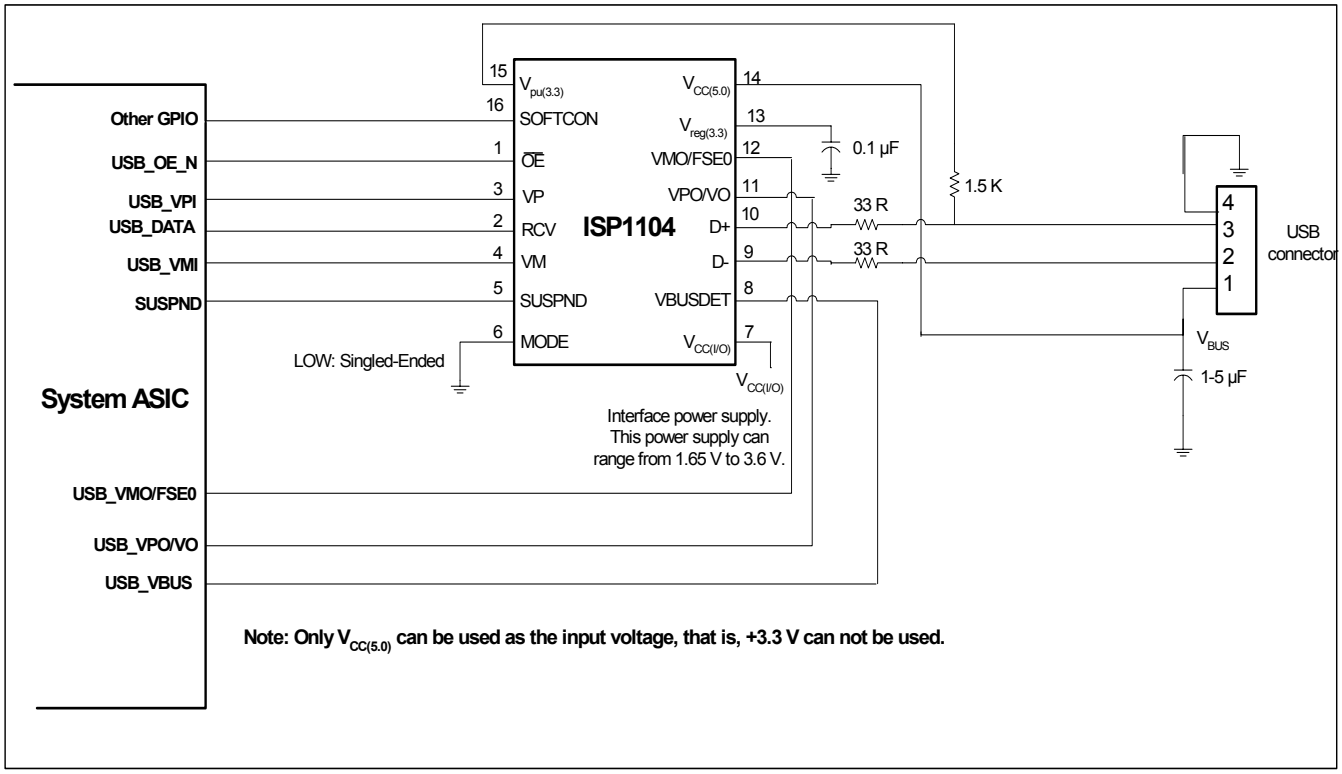

Figure 3-1: Upstream Connection with the ISP1104 in the Singled-Ended Mode

Figure 3-2 shows a typical schematic of the upstream connection with the ISP1104 in the differential mode.

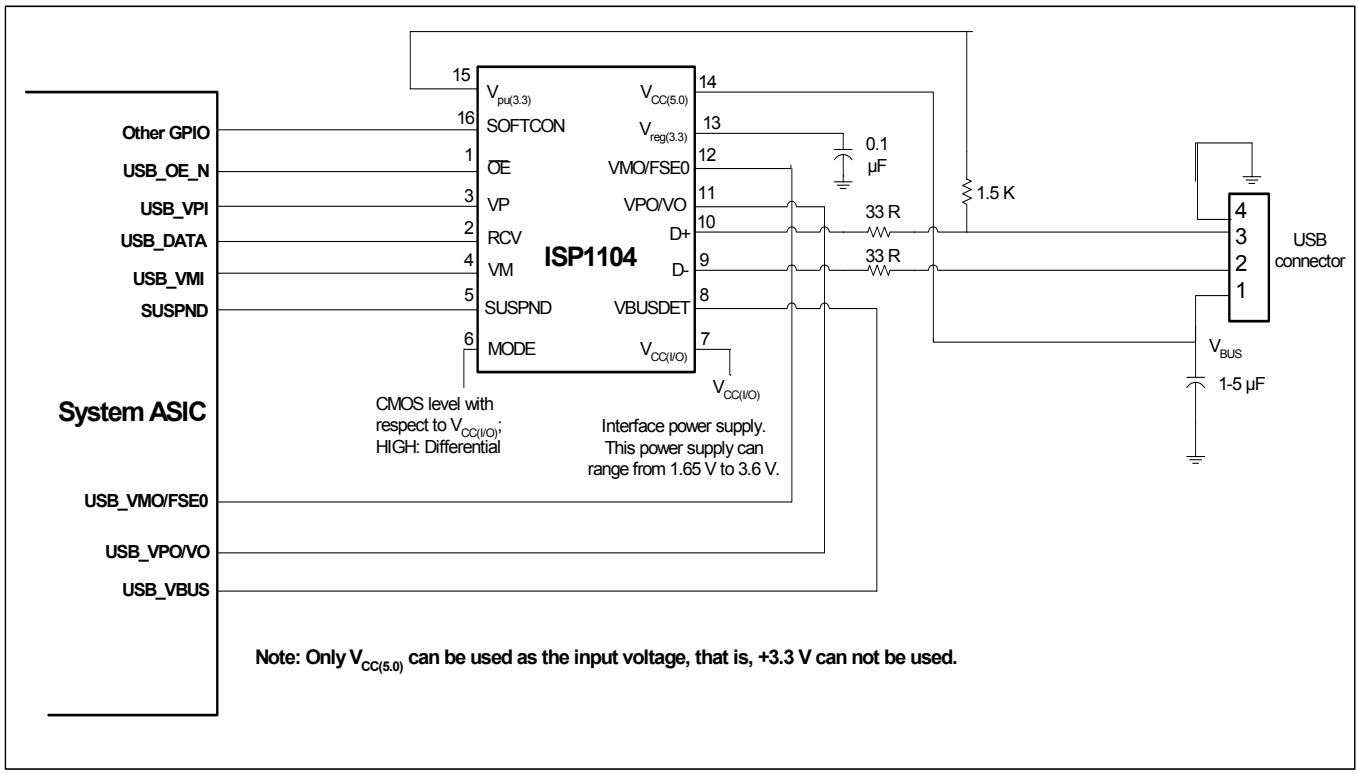

Figure 3-2: Upstream Connection with the ISP1104 in the Differential Mode

The upstream port connection can be done by pulling up the 1.5 kΩ resistor on D+ and D– by using $V_{pu(3.3)}$. Use the SOFTCON pin to enable or disable the pull-up.

$V_{CC(I/O)}$ is provided by the backend, FPGA or general microcontroller board circuitry. This voltage can range from 1.65 V to 3.6 V.

For the downstream port connection, leave $V_{pu(3.3)}$ open. There is no 1.5 kΩ pull-up resistor from the D+ and D– lines to $V_{pu(3.3)}$. There are, however, two 15 kΩ termination resistors on the D+ and D– lines to GND. To reduce power consumption, short the SOFTCON pin to GND.

Figure 3-3 provides a typical schematic of the downstream connection with the ISP1104 in the single-ended mode.

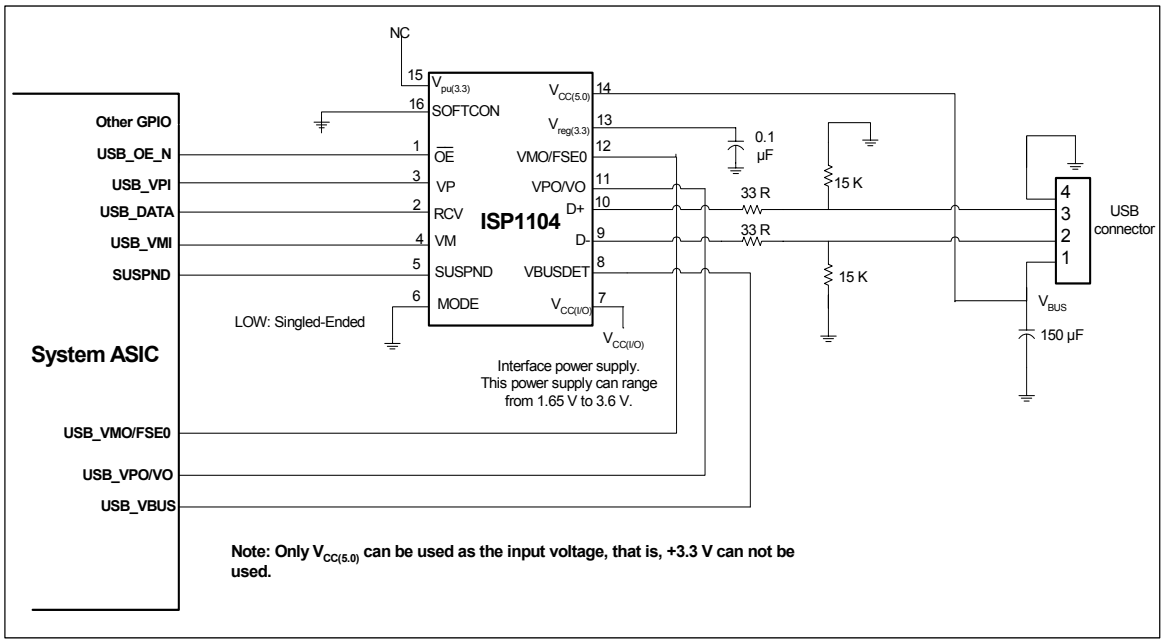

Figure 3-3: Downstream Connection with the ISP1104 in the Single-Ended Mode

Figure 3-4 shows a typical schematic of the downstream connection with the ISP1104 in the differential mode.

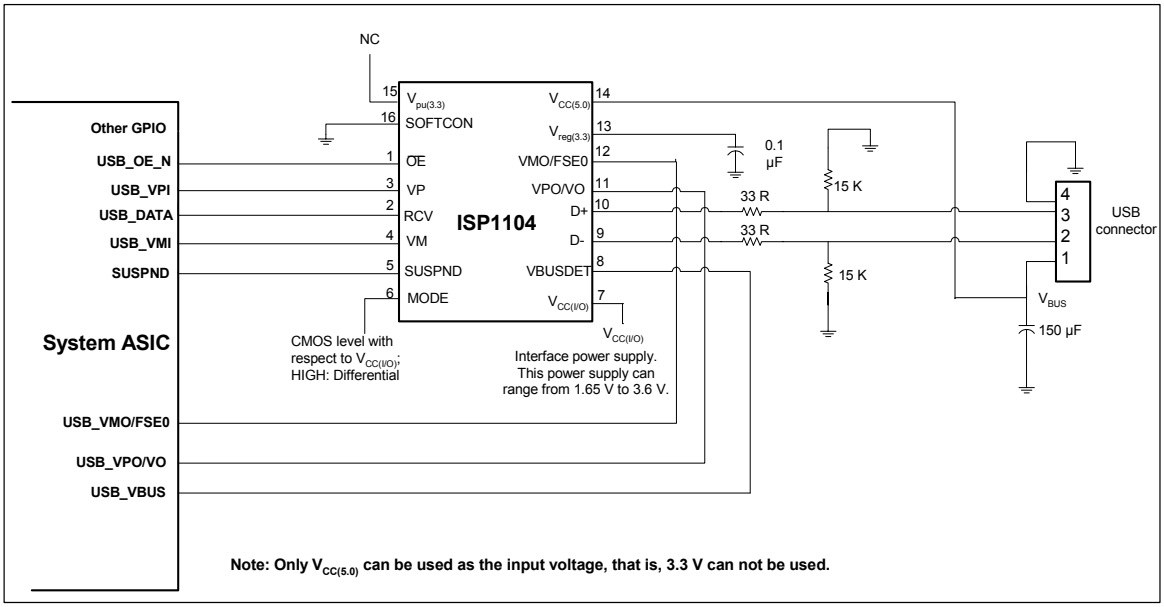

Figure 3-4: Downstream Connection with the ISP1104 in the Differential Mode

Note: The pin assignment for the ISP1104W (HBCC16) and the ISP1104BS (HVQFN16) is the same.

4. ISP1105; ISP1106

4.1. Features of the ISP1105; ISP1106

- Compliant with ***Universal Serial Bus Specification Rev. 2.0.***
- Can transmit and receive USB data at full-speed (12 Mbit/s) or low-speed (1.5 Mbit/s).
- Support I/O voltage range from 1.65 V to 3.6 V.
- The MODE input pin allows selection between single-ended and differential input modes.
- Available in small HBCC16, HVQFN16 (only ISP1105) and TSSOP16 (only ISP1106) packages; HBCC16 and HVQFN16 are lead-free and halogen-free packages.

In the sharing mode, $V_{CC\ (I/O)}$ is connected. $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are not connected. In this mode, the D+ and D– pins are made three-state and the ISP1105; ISP1106 allow external signals of up to 3.6 V to share the D+ and D– lines. The internal circuits ensure that virtually no current (maximum 10 A) is drawn through the D+ and D– lines. The power consumption through $V_{CC(I/O)}$ drops to the low-power (suspend) state level. The VP and VM pins are driven HIGH and the RCV pin is made LOW to indicate this mode.

4.2. Interfacing the ISP1105W; ISP1106W to a System ASIC

Under +3.3 V operation environment

Figure 4-1 provides a typical schematic of the upstream connection circuitry with the ISP1105W; ISP1106W under 3.3 V environment.

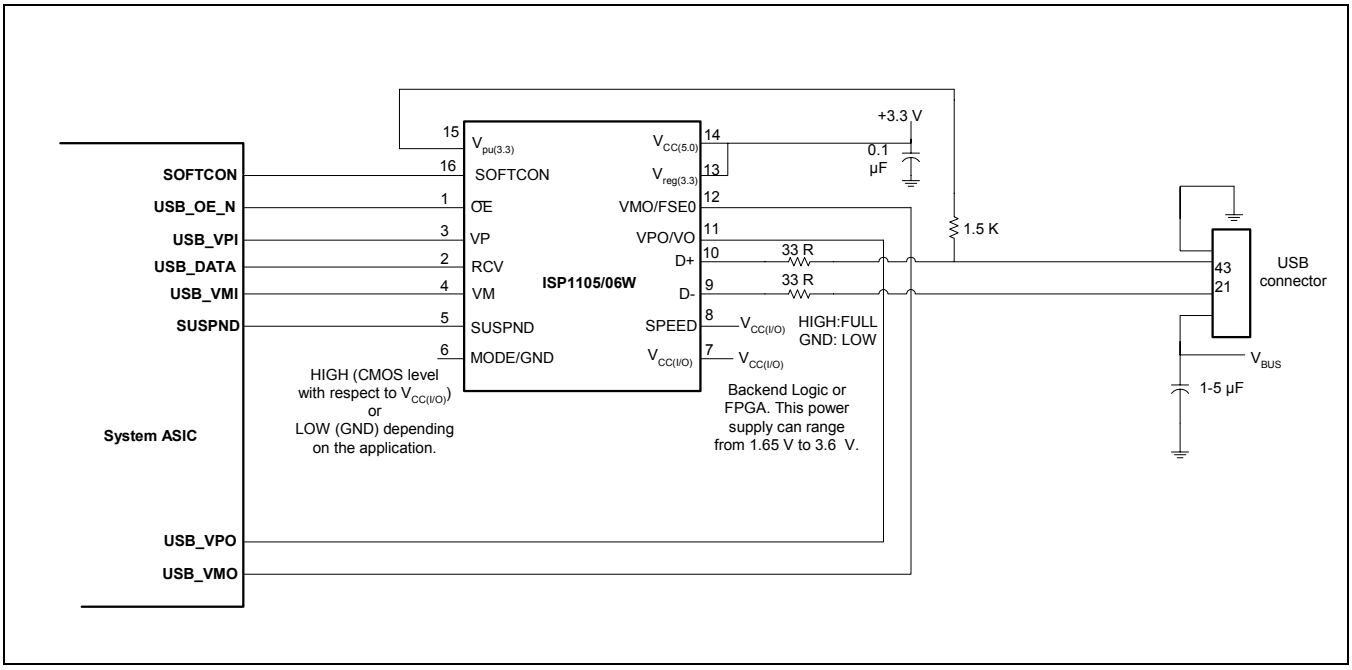

Figure 4-1: Upstream Connection with the ISP1105W; ISP1106W under 3.3 V Environment

When the supply voltage is 3.3 V, $V_{CC(5.0)}$ and $V_{reg(3.3)}$ must be shorted together to bypass the 5.0-to-3.3 V regulator. You can connect the upstream port by using a 1.5 kΩ resistor on D+ for full-speed (12 Mbit/s) or a 1.5 kΩ resistor on D– for low-speed (1.5 Mbit/s). This resistor can be pulled up by using $V_{pu(3.3)}$. Use the SOFTCON pin to enable or disable the pull-up.

$V_{CC(I/O)}$ is provided by the backend or FPGA circuitry. This voltage can range from 1.65 V to 3.6 V.

For the downstream port connection, leave $V_{pu(3.3)}$ open. There is no 1.5 kΩ resistor from the D+ and D– lines to $V_{pu(3.3)}$. There are, however, two 15 kΩ resistors from the D+ and D– lines to GND. Short the SOFTCON pin to GND (LOW) to reduce power consumption.

A typical schematic of the downstream connection circuitry with the ISP1105W; ISP1106W under 3.3 V environment is given in Figure 4-2.

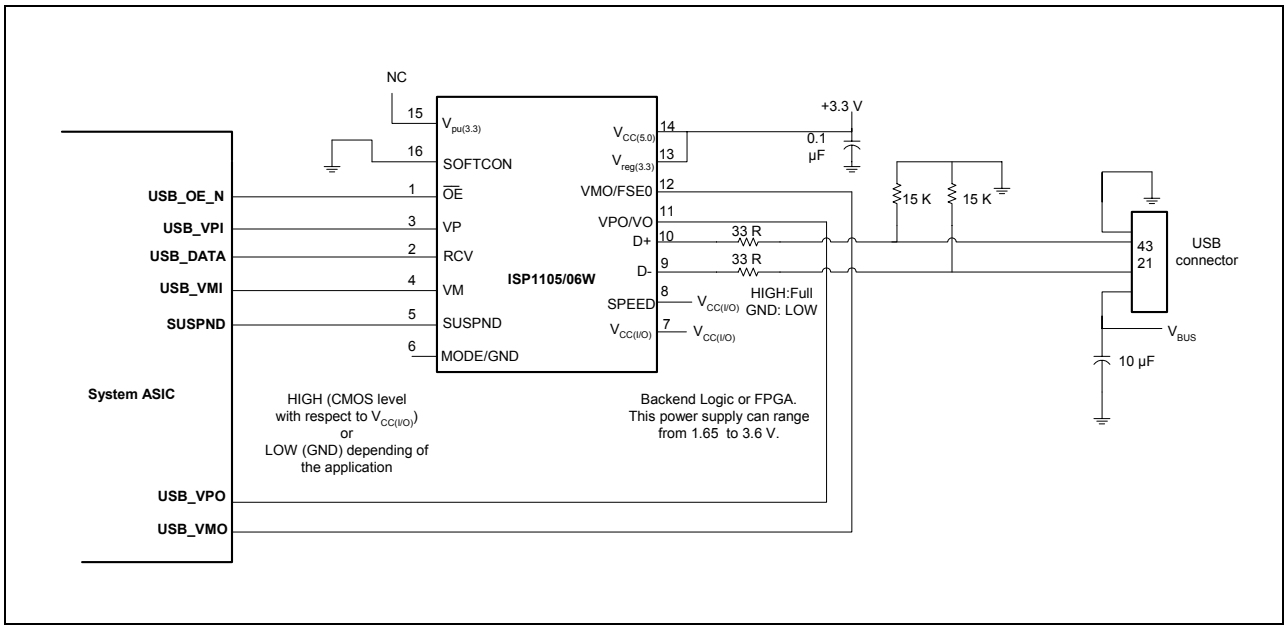

Figure 4-2: Downstream Connection with the ISP1105W; ISP1106W under 3.3 V Environment

Under +5.0 V or V_{BUS} operation environment

Figure 4-3 shows a typical schematic of the upstream connection circuitry with the ISP1105W; ISP1106W under 5.0 V environment:

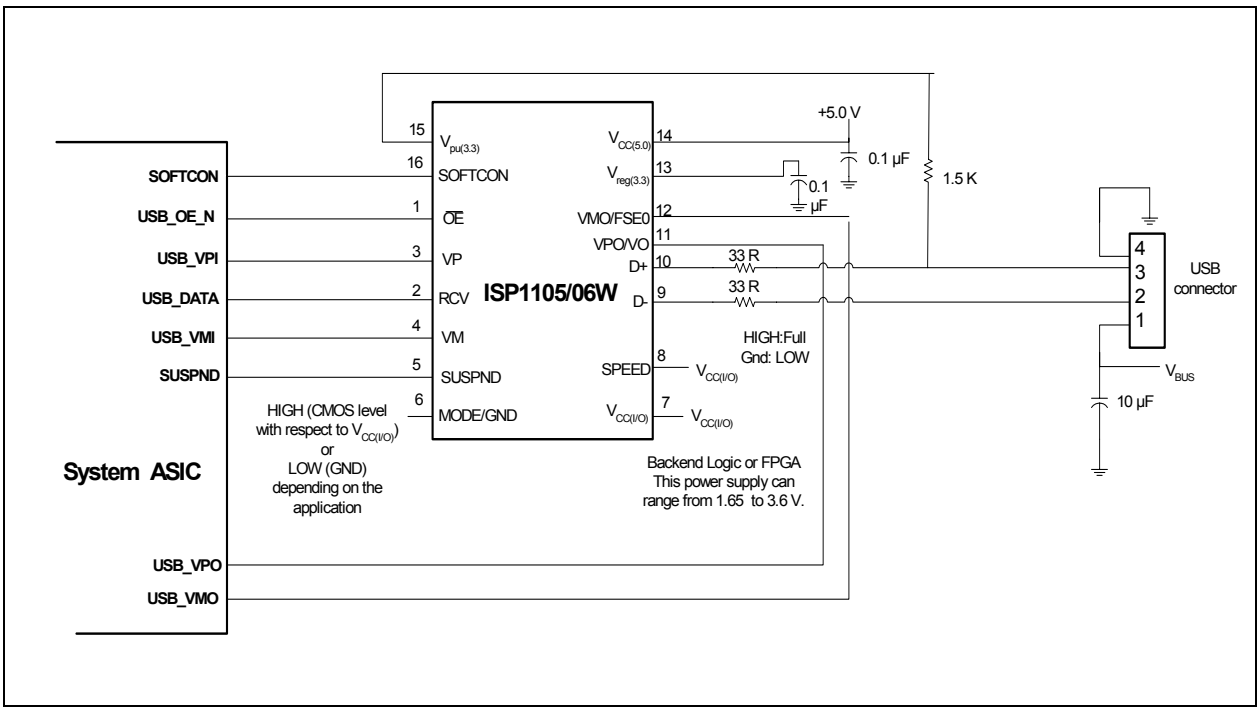

Figure 4-3: Upstream Connection with the ISP1105W; ISP1106W under 5.0 V Environment

In Figure 4-3, $V_{CC(5.0)}$ is 5.0 V (from the backend logic or V_{BUS}) and $V_{CC(I/O)}$ is the backend or FPGA logic power supply (ranges from 1.65 V to 3.6 V). $V_{reg(3.3)}$ must be connected to a decoupling capacitor of 0.1 F, which is connected to GND.

A typical schematic of the downstream connection circuitry with the ISP1105W; ISP1106W under 5.0 V environment is given in Figure 4-4.

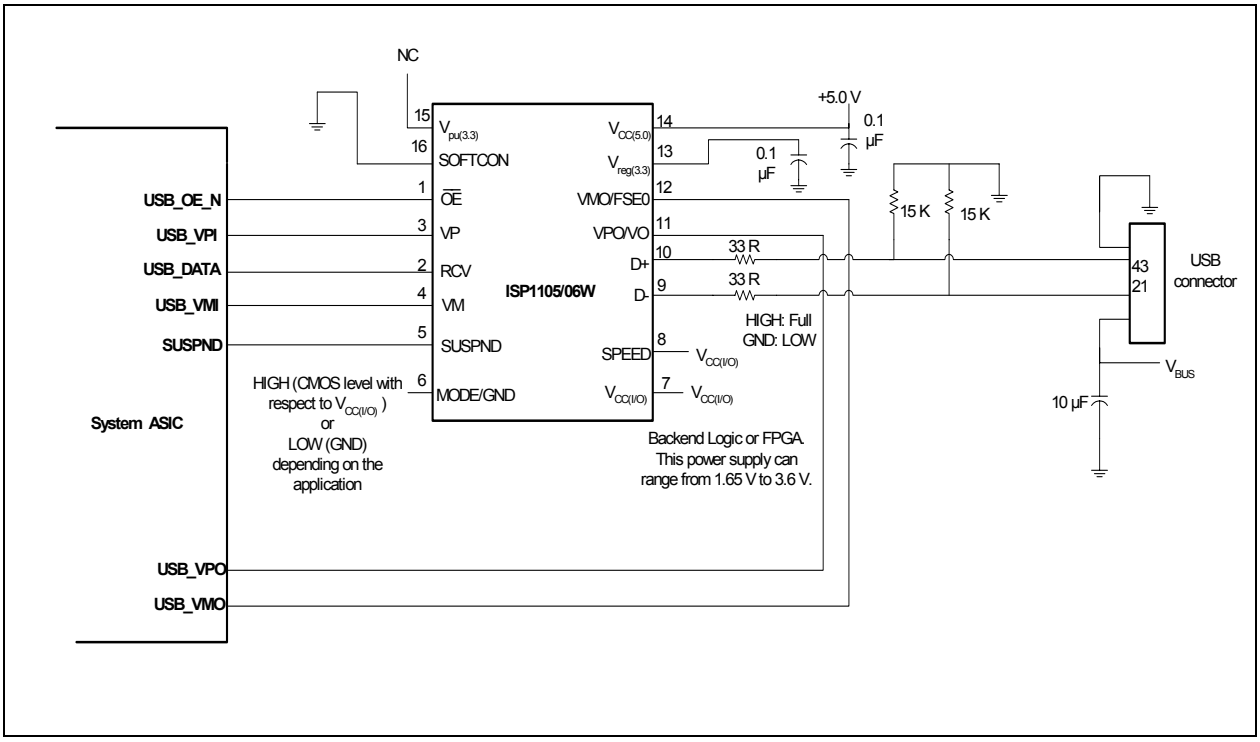

Figure 4-4: Downstream Connection with the ISP1105W; ISP1106W under 5.0 V Environment

Figure 4-1 to Figure 4-4 provide the connection circuitry for ISP1105W and ISP1106W (HBCC16 package). If you are using the HVQFN16 or TSSOP16 package in your application, see Table 4-2 for the pin assignment.

Table 4-1: Pin Assignment for the TSSOP16 and HVQFN16 Packages

Pin No	TSSOP16 (ISP1106DH)	HVQFN16 (ISP1105BS)
1	$V_{pu(3.3)}$	$\overline{OE}$
2	SOFTCON	RCV
3	$\overline{OE}$	VP
4	RCV	VM
5	VP	SUSPND
6	VM	MODE
7	SUSPND	$V_{CC(I/O)}$
8	GND	SPEED
9	$V_{CC(I/O)}$	D–
10	SPEED	D+
11	D–	VPO/VO
12	D+	VMO/FSE0
13	VPO/VO	$V_{reg(3.3)}$
14	VMO/FSE0	$V_{CC(5.0)}$
15	$V_{reg(3.3)}$	$V_{pu(3.3)}$
16	$V_{CC(5.0)}$	SOFTCON

4.3. Mode Selections and Configurations Used in the ISP1105; ISP1106

Table 4-2: ISP1105; ISP1106 Mode Selections and Configurations

IC Products and Packages[1][2]	Pin Mode	Operation Mode	Remark (For Backend Logic or FPGA)[3]
ISP1105W	Short (Pin 6–GND)	Single-Ended Input Mode (VO, FSE0)	Singled-Ended Input Logic
	Open (Pin 6–HIGH)	Differential Input Mode (VPO, VMO)	Differential Input Logic
ISP1106W	Short (Pin 6–GND)	Differential Input Mode (VPO, VMO)	Differential Input Logic
ISP1106DH	Short (Pin 8–GND)	Differential Input Mode (VPO, VMO)	Differential Input Logic

[1] If you are using a different package, refer to the ISP1105_1106 data sheet.
[2] W denotes the HBCC16 IC package; DH denotes the TSSOP16 IC package.
[3] The backend logic circuitry must be compatible to the operation mode.

For the ISP1106DH package pinning information, refer to the ISP1105_1106 data sheet. The pin interface connection is the same as that for the W type (HBCC) package.

Section 4.4 provides examples on interfacing the ISP1105W and the ISP1106W to QUALCOMM® MSM51xx or MSM31xx.

4.4. Interfacing the ISP1105W and the ISP1106W to QUALCOMM MSM Chipset

Figure 4-5 and Figure 4-6 provide example schematics on interfacing the ISP1105W and the ISP1106W, respectively, to the QUALCOMM MSM™ chipset in mobile phone applications.

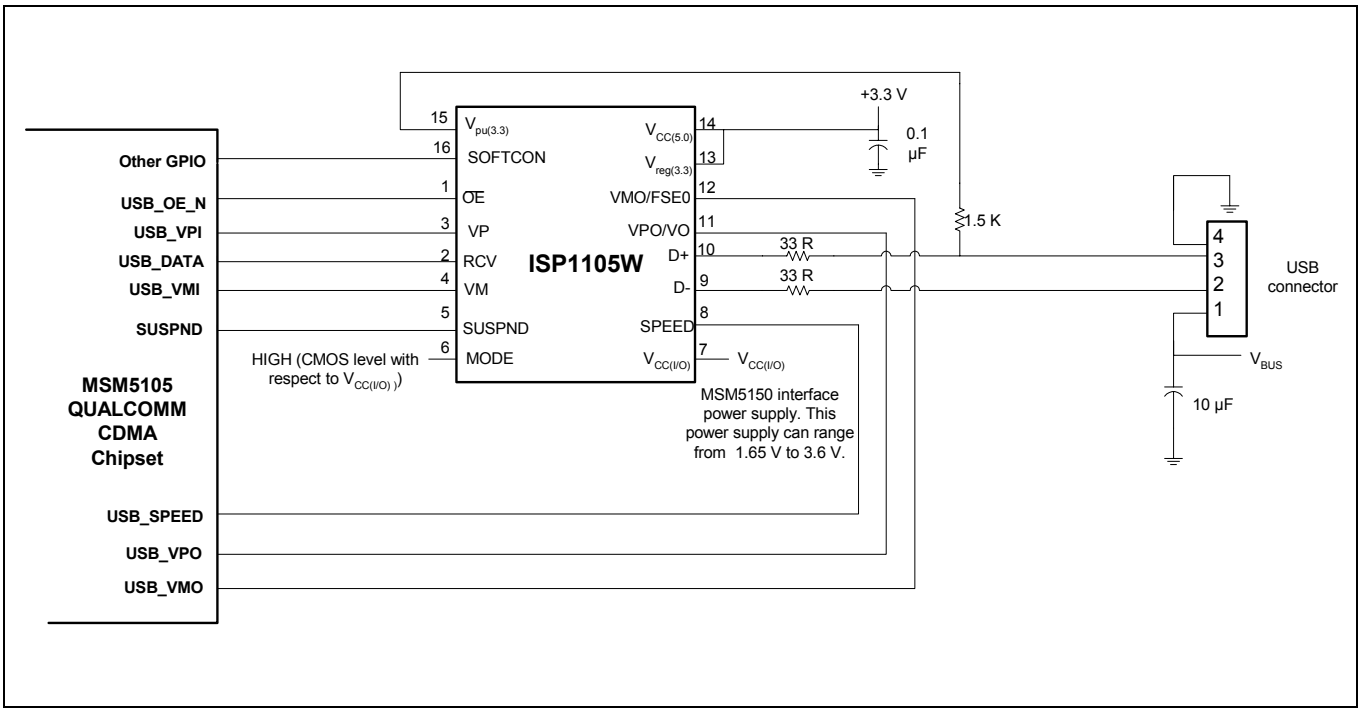

Figure 4-5: Upstream Connection with the ISP1105W under 3.3 V Environment

Figure 4-5 shows:

- The MSM5105™ interfacing circuit provides $V_{CC(I/O)}$. This voltage can range from 1.65 V to 3.6 V.
- The MODE pin (pin 6) of the ISP1105W must be connected to HIGH to support the differential input mode and connected to LOW to support the single-ended input mode.
- The SPEED pin can be pulled up from the chipset either by using USB_SPEED or by using a weak pull-up resistor (10 kΩ) for full-speed.

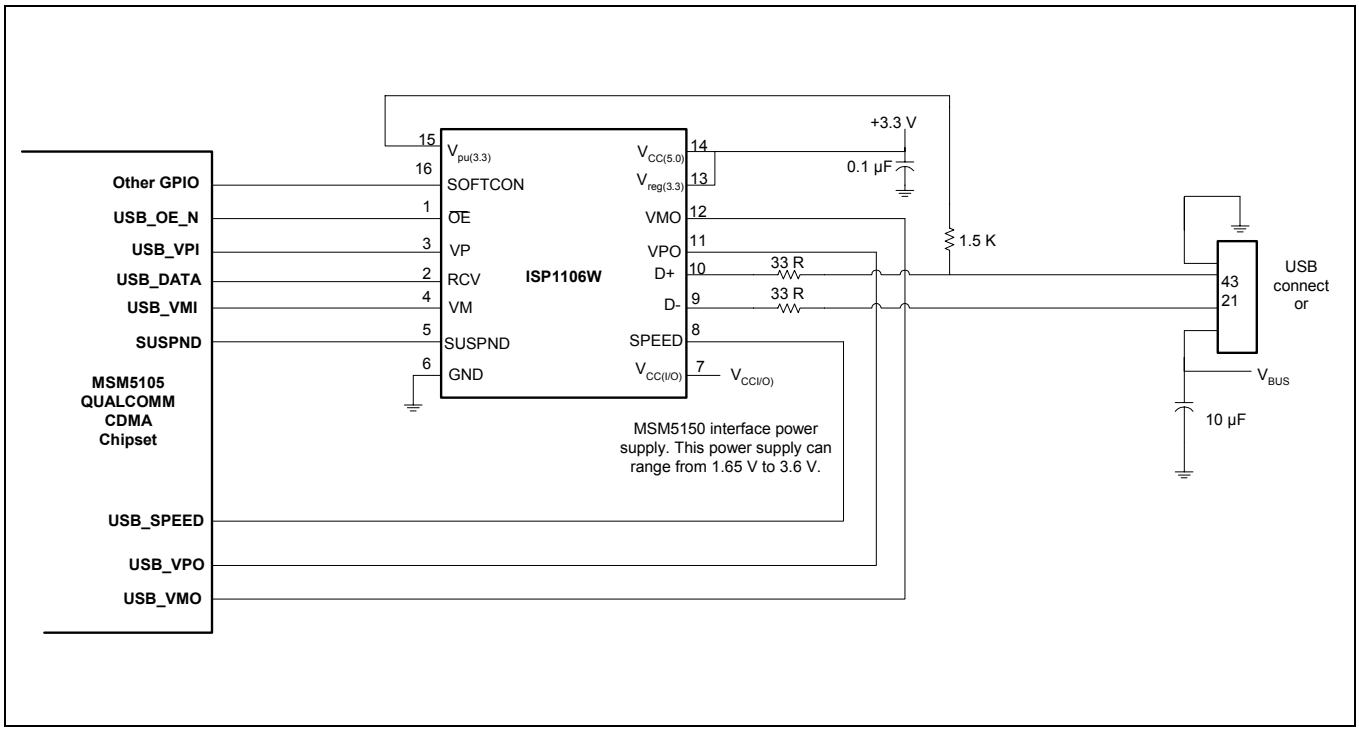

Figure 4-6: Upstream Connection with the ISP1106W under 3.3 V Environment

Figure 4-6 shows the GND pin (pin 6) of the ISP1106W is shorted to ground (LOW).

When using the ISP1106DH, refer to the ISP1105_1106 data sheet for the pin configuration. The application circuitry is the same as that of the ISP1106W.

5. General Design Precautions

- The $V_{reg(3.3)}$ pin must not be left open. It must be connected to a 0.1 F capacitor, which is connected to GND.
- A weak pull-up resistor can be used for the SPEED and MODE pins or the pins that must be pulled HIGH.
- The $V_{CC(5.0)}$ pin of the ISP1105; ISP1106 cannot detect V_{BUS} lost, which is possible in the ISP1104 . For details, refer to the respective data sheets.
- The sharing mode is not the suspend mode. Therefore, during the sharing mode, to reduce power consumption and to go into suspend, the SUSPND pin can be pulled HIGH. To ensure that the IC is in the suspend mode:
  - For ISP1105; ISP1106: make sure that the VP and VM pins are driven HIGH and the RCV pin is LOW.
  - For ISP1102 and ISP1104: make sure that the VP/VPO and VM/VMO pins are driven HIGH, and the VBUSDET and RCV pins are driven LOW.

- Do not operate the ISP1104 under +3.3 V environment or in the regulator bypass mode. This is because the $V_{CC(5.0)}$ pin is used for the V_{BUS} detection. This pin must be connected to the V_{BUS} line of the USB connector.
- Connect a decoupling capacitor of 1 F to 10 F to $V_{CC(5.0)}$ (which is directly connected to the V_{BUS} line).

6. References

- ***Universal Serial Bus Specification Rev. 2.0***
- ***ISP1102 Advanced Universal Serial Bus transceiver*** data sheet
- ***ISP1104 Advanced Universal Serial Bus transceiver*** data sheet
- ***ISP1105_1106 Advanced Universal Serial Bus transceivers*** data sheet.